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PATENT APPLICATION

SEMICONDUCTOR PROCESS CHAMBER ELECTRODE AND METHOD FOR MAKING THE SAME

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BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to semiconductor fabrication equipment, and more particularly, the present invention relates to improved semiconductor processing chamber electrodes and methods for making and implementing the improved electrodes.

2. Description of the Related Art

In semiconductor fabrication, integrated circuit devices are fabricated from semiconductor wafers that are placed through numerous processing operations. Many of the numerous processing operations are commonly carried out in processing chambers in which layers, such as, dielectric and metallization materials are successively applied and patterned to form multi-layered structures. For example, some of these layers (*e.g.*, SiO₂) are commonly deposited in chemical vapor deposition (CVD) chambers, and then photoresist materials are spin-coated and placed through photolithography patterning. When a photoresist mask is defined over a particular surface, the semiconductor wafer is placed into a plasma etching chamber in order to remove (*i.e.*, etch) portions of the underlying materials that are not covered by the photoresist mask.

Figure 1A shows a semiconductor processing system 100 including a chamber 102 that is used for processing semiconductor wafers through etching operations. In

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this example, the chamber 102 includes a chuck 104 which is configured to support a semiconductor wafer 106. The chuck 104 also supports a plurality of quartz rings 108. Over a topmost quartz ring 108, sits a ceramic ring holder 110, which is configured to hold a top electrode 114. The top electrode 114 is configured to receive
5 processing gases which will be distributed into the plasma region 112 during processing.

The top electrode is also shown coupled to a match box and diplexer 116a and an RF power source 118a. The chuck 104 is also coupled to a match box and diplexer 116b and an RF power source 118b. The chamber 102 is provided with outlets 120
10 which are configured to pump out excess gases from within the chamber during processing. In operation, the RF power supply 118a is configured to bias the top electrode 114 and operate at frequencies of about 27 MHz. The RF power source 118a is primarily responsible for generating most of the plasma density within the plasma region 112, while the RF power source 118b is primarily responsible for
15 generating a bias voltage within the plasma region 112. The RF power source 118b generally operates at lower frequencies in the range of about 2 MHz.

Figure 1B provides a more detailed view of the top electrode 114 of the semiconductor processing system 100. The top electrode 114 generally includes a number of gas buffer plates 122 which have a plurality of holes defined throughout
20 their surface region, and are configured to evenly distribute the processing gases throughout the top electrode 114. In this manner, the gas buffer plates 112 will ensure that an about equal amount of gas is allowed to flow out of each of the gas feed holes 128 of a silicon plate 126. The top electrode 114 also has a graphite ring 124 which is configured to mount onto the ceramic holders 110 of Figure 1A. Once

the process gases are allowed to flow out of the gas feed holes 128, a plasma may be generated in the plasma region 112 that is defined between the surface of the silicon plate 126 and a surface of the wafer 106.

During operation, the RF power 118a and the RF power 118b is applied to the top electrode 114 and the chuck 104, respectively. Once the process gases are channeled into the top electrode 114 and allowed to flow out of the gas feed holes 128 into the plasma region 112, a plasma sheath 131 and 132 will be defined within the plasma region 112 as shown in Figure 1C.

As pictorially shown, the silicon plate 126 will have an electrode surface 134 which is directly opposite a wafer surface 136 of the semiconductor wafer 106. As is well understood in plasma physics, the electrode surface 134 and the wafer surface 136 are partially responsible for producing the plasma sheaths 131 and 132 within the plasma region 112.

Specifically, as shown in Figure 1D, plasma sheaths edges are defined at points 133a and 133b along a plasma density profile 133. The plasma density profile illustrates that the plasma concentration falls to about zero near the wafer surface 136 and the top electrode surface 134. As such, the plasma concentration gradually increases from zero up to a constant concentration between points 133a and 133b. The electrode surface 134 and the wafer surface 136 will therefore ensure that the bulk of the plasma is contained between the plasma sheaths 131 and 132 as shown in Figure 1C.

As the demand to etch smaller and smaller integrated circuit device patterns continues to increase, more difficult high aspect ratio etching will be needed. As

shown in Figure 1E, a cross sectional view 140 of a wafer substrate 106' is shown.

The wafer substrate 106' has a dielectric layer 140 deposited thereon and a patterned photoresist layer 142. The photoresist layer 142 has a patterned window 144 defining a window down to the dielectric layer 140. As the aspect ratios continue to increase

5 (i.e., deeper and narrower etching geometries), a process window that defines a set of controllable process parameters will also rapidly shrink. When the process window shrinks, adjustment of process parameters will no longer improve etch rates, etch selectivities, or etch profiles.

Typically, the process parameters include pressure settings, flow rates,
10 electrode biasing powers, types of processing chemistries, and so on. However, as aspect ratios continue to increase, varying the process window parameters no longer assist a processing chamber's ability to control a desired etching operation. For example, when a geometry such as that defined by the patterned window 144 (i.e., for a contact via or the like) in the photoresist layer 142 is desired, the best etching
15 chemistries may no longer be able to etch all the way down through the dielectric layer 140. When that happens, a premature etch stop 146 will develop because the processing chemistries will also be depositing polymers on the sidewalls and the bottom during the etching operation. As is well known, this polymer deposition can seriously retard the etching of dielectric layers 140 when high aspect ratio patterns are
20 the subject of etching.

In efforts to combat this problem, process engineers have in the past, attempted to increase the level of oxygen within the processing chamber during an etch operation. Unfortunately, when the oxygen level is increased within the processing chamber, the etching operation will produce a bow-shaped etch 148 within

the dielectric layer 140. As can be appreciated, when such a bow-shaped etch 148 occur within the dielectric layer 140, subsequent filling of the via hole defined by the bow-shaped etch 148 will be problematic. That is, conventional conductive fill techniques used to deposit metallization within a via hole may not work because of the bow-shaped etch via 148. As a result, a fabricated device having the bow-shaped etch via holes 148 may fail to function within its intended design.

Another solution attempted in the prior art has been to increase the bias power of the RF power source 118b that is coupled to the chuck 104 in an attempt to increase the ion bombardment energy over the surface of the wafer 106. However, when the bias voltage of the RF power source 118b is increased, more plasma is also generated within the plasma region 114, which counteracts the increase in ion bombardment energy. In addition, the processing molecules channeled into the plasma region 112 may change their chemical composition when the bias power is increased, and therefore, may fail to perform the desired etching. Consequently, it has been observed that merely increasing the RF power that is applied to the chuck 104 does not help in improving the etching of high aspect ratio geometries.

In view of the foregoing, what is needed is a processing apparatus and method for making and implementing the apparatus which will assist in increasing the ion bombardment energy at the surface of a wafer without also increasing the plasma density or changing the chemical composition of the processing molecules.

SUMMARY OF THE INVENTION

The present invention fills these needs by providing a semiconductor processing chamber electrode that assists in shifting an increased ion bombardment energy toward the surface of the semiconductor wafer. It should be appreciated that
5 the present invention can be implemented in numerous ways, including as a process, an apparatus, a system, a device, and a method. Several inventive embodiments of the present invention are described below.

In one embodiment, a system for processing a semiconductor wafer through plasma etching operations is disclosed. The system has a process chamber that
10 includes a support chuck for holding the semiconductor wafer and a pair of RF power sources. The system further includes an electrode that is positioned within the system and over the semiconductor wafer. The electrode has a center region, a first surface and a second surface. The first surface is configured to receive processing gases from a source that is external to the system and flow the processing gases into the center
15 region. The second surface has a plurality of gas feed holes that are continuously coupled to a corresponding plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes. The plurality of electrode openings are configured to define an electrode surface that is defined over a wafer surface of the semiconductor wafer. The
20 electrode surface assists in increasing an electrode plasma sheath area in order to cause a shift in bias voltage onto the wafer surface, thereby increasing the ion bombardment energy over the wafer without increasing the plasma density.

sheath has a greater surface area than the substantially planar first plasma sheath. The greater surface area therefore causes an increased bias voltage over the wafer surface and a decreased bias voltage over the electrode surface.

Advantageously, it is now possible to increase the bias voltage over the surface of the wafer without also causing an increase in plasma density. Because an increased bias voltage is essentially an increase in ion bombardment energy, higher aspect ratio geometries can now be etched without causing premature etch stops or bow etch profiles. These and other advantages of the present invention will become apparent upon reading the following detailed descriptions and studying the various figures of the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention, together with further advantages thereof, may best be understood by reference to the following description taken in conjunction with the accompanying drawings.

5 Figure 1A shows a semiconductor processing system including a chamber that is used for processing semiconductor wafers through etching operations.

Figure 1B provides a more detailed view of a top electrode of a semiconductor processing system.

10 Figure 1C shows a plasma and plasma sheaths formed next to an electrode surface and a wafer surface.

Figure 1D shows a plasma concentration profile and the plasma sheath locations relative to an electrode surface and a wafer surface.

Figure 1E shows a cross sectional view of a semiconductor substrate undergoing an etch operation.

15 Figure 2A shows a cross sectional view of a top electrode in accordance with one embodiment of the present invention.

Figure 2B shows a plan view of a surface of the electrode body in accordance with one embodiment of the present invention.

20 Figure 2C shows a more detailed view of the electrode opening of Figure 2A in accordance with one embodiment of the present invention.

Figure 2D shows an alternative detailed view of an electrode opening in accordance with one embodiment of the present invention.

Figure 2E shows a more detailed view of the electrode opening surfaces, a wafer surface, and a corresponding plasma having plasma sheaths in accordance with one embodiment of the present invention.

Figure 3 shows a more detailed view of a contoured plasma sheath that is defined into the electrode openings and a substantially planar plasma sheath that is defined over the wafer surface in accordance with one embodiment of the present invention.

Figure 4A shows voltage waveforms plotted over time, including a shifted voltage waveform that causes a shift in bias voltage in accordance with one embodiment of the present invention.

Figure 4B shows a graph illustrating the resulting current magnitudes over a cycle of a shifted voltage waveform of Figure 4A in accordance with one embodiment of the present invention.

Figure 5 is a graph illustrating bias vs. area ratio for the plasma sheaths of a top electrode and a wafer in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

An invention is described for a semiconductor processing chamber electrode that assists in shifting an increased plasma ion bombardment energy toward the surface of the semiconductor wafer to improve etching of high aspect ratio geometries. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be obvious, however, to one skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process steps have not been described in detail in order not to unnecessarily obscure the present invention.

As described above, the present invention discloses a unique top electrode that enables processing chambers to retain control of processing windows during high aspect ratio etching operations. Although the top electrodes of the present invention can be implemented into many different types of processing chambers, one exemplary chamber that will benefit from the inventive design features of the disclosed top electrodes is a Lam Research Rainbow 4520XL processing chamber, which is available from Lam Research Corporation of Fremont, California. In some chamber orientations, the top electrode may be grounded and both frequencies are fed to the bottom electrode (i.e., wafer support chuck). In either case, the top electrode configuration of the present invention will assist in increasing the ion bombardment energy on the surface of the wafer without the side effects of the prior art.

Figure 2A shows a cross sectional view of a top electrode 200 in accordance with one embodiment of the present invention. In this embodiment, the top electrode

200 includes an electrode body 202 that has a plurality of electrode regions 202c that define respective electrode openings 202b. The electrode openings 202b form a channel that leads to a plurality of gas feed holes 228. In general, the gas feed holes 228 channel the processing gases to a plasma region 112, as described with respect to Figure 1A. Accordingly, when the top electrode 200 is inserted into a semiconductor processing system chamber, a surface 234 of the electrode body 202 will define the surface that is in close proximity to a generated plasma sheath.

In a preferred embodiment of the present invention, the inter-portion of the electrode body 202 will preferably have an opening 250 which is about the same diameter of a wafer being processed. For example, when an 8-inch wafer is being processed, the diameter 250 is preferably sized to be about 8 inches. Although not shown, gas buffer plates are typically positioned within the electrode body 202. The electrode body 202 has a preferred thickness 252 of about 1 inch, while the electrode regions 202c have a thickness 256 that is about ¼ inch. Of course, these exemplary dimensions may be modified depending on the size of the semiconductor wafer being processed.

Figure 2B shows a plan view of the surface 234 of the electrode body 202 in accordance with one embodiment of the present invention. As shown, the electrode openings 202b are preferably arranged throughout the surface 234 in a hexagonal pattern arrangement. In this hexagonal pattern arrangement, the separation 203 between the electrode openings 202b is preferably set to about 0.375 inches. Also, in a preferred embodiment, the diameter of each of the electrode openings 202b is set to be about 0.25 inches.

Figure 2C shows a more detailed view of the electrode opening 202b of Figure 2A in accordance with one embodiment of the present invention. The electrode opening 202b has a diameter D_3 242 that is selected to be at least equal to or greater than about $5 \Lambda_{\text{Debye}}$ (*i.e.*, ≥ 0.5 mm). The depth D_4 244 of the electrode opening 202b is preferably set to be between about 1/32 inch and about 1/4 inch, and more preferably between about 1/16 inch and about 1/4 inch, and most preferably about 1/8 inch. Preferably, the diameter D_2 240 is about 0.1 mm. In this embodiment, the electrode opening 202b has an angled (about 30 degrees) surface 246, which is caused by the profile of a machining drill bit. However, it should be understood that other angles will work as well. For example, Figure 2D shows a case in which the angled surface 246 is replaced with a right angle 248. Of course, when the angled surface 246 is removed, the electrode opening 202b may extend to a distance D_5 249, which may be greater than distance D_4 244.

Figure 2E shows a cross sectional view of three electrode regions 202c and a cross section of the wafer 206 in accordance with one embodiment of the present invention. In a preferred embodiment, the distance between the surface 234 and the wafer surface 236 is preferably set to be between about 0.75 cm and about 4 cm, and more preferably between about 1 cm and about 3 cm, and most preferably about 2 cm. Once the semiconductor processing system is placed into its operational state (*i.e.*, processing gases have been flown into the chamber, biasing powers have been set, pressures and temperatures adjusted, etc.), a plasma is generated within a plasma region 212. Because the electrode openings 202b have been increased to be at least equal to or greater than about $\frac{1}{\Lambda} 5$ mm, a plasma sheath 231 is caused to shift into the electrode openings 202b.

As pictorially shown, the shifted plasma sheath 231 follows the profile of the electrode opening 202b walls. That is, the plasma sheath 231 is separated from the surface 234 and electrode opening surfaces 204 by a distance D_1 , 233. In one embodiment, the distance D_1 , 233 may be between about 0.5 mm, and about 5 mm, and most preferably about 2 mm. Because the plasma sheath next to the top electrode in prior art designs is not shifted as shown in Figure 1C, the surface area of both plasma sheaths will be about equal. However, because the plasma sheath 231 is shifted into the electrode openings 202b throughout the top electrode 200, the surface area of the plasma sheath 231 will be greater than the surface area of the plasma sheath 232.

Figure 3 shows a cross sectional view of the plasma sheath 231 that conforms to the surfaces of the electrode regions 202c as shown in Figure 2E, and the plasma sheath 232 that is defined above the wafer 206. Although only a cross sectional view of the sheaths 231 and 232 are shown, it should be understood that the sheaths are actually three-dimensional (3D) blankets that are defined over each of the surfaces of the top electrode 200 and the wafer 206. As such, a substantial increase in sheath area₁ is produced when the sheath 231 shifts into the electrode openings 202b. Table A below shows an exemplary calculation of the increase in sheath 231 surface area₁ compared to the sheath 232 surface area₂. Of course, other area increases may be obtained depending on the specific electrode opening geometries.

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increase as shown in Figure 3. At this point, the magnitude of current (ion and electron current) flowing through the plasma will be different during the time that a current I_1 flows away from the wafer 206 in the direction of the top electrode 200 and during the time that a current I_2 flows away from the top electrode 200 in the direction of the wafer 206. In fact, because there is a greater sheath surface area close to the top electrode surface 234/204, the current I_1 will have a greater magnitude than the current I_2 as depicted in Figure 3.

Because of this current magnitude difference, the sinusoidal voltage wave 302 will shift downward to form a shifted sinusoidal voltage wave 302'. At this point, it should be evident that the shifted sinusoidal voltage wave 302' will be positive for a shorter amount of time T_1 than it is negative T_2 . However, over a full cycle, the current flowing in one direction (i.e., I_1) across the plasma has to be the same as the current flowing in the other direction (i.e., I_2). Figure 4B illustrates how a total current during time T_1 for the larger magnitude current I_1 will actually equal a total current during a time T_2 for a smaller magnitude current I_2 . Specifically, the area under 320a defines the net current for I_1 and the area under 320b defines the net current for I_2 . For reference purposes only, the net current under area 310a and 310b are also equal to each other in a non-shifted system.

Referring back to Figure 4A, a wave portion 306 is the result of a half-wave rectification that is induced by the generated plasma. When a time average is taken over one cycle of the wave portion 306, a bias voltage on the surface of the top electrode is produced. In a like manner, a wave portion 308 is the result of another half-wave rectification that was induced by the generated plasma. Upon taking a time average over one cycle of the wave portion 308, a bias voltage on the surface of the

wafer is produced. It is important to note that the bias voltage produced on the surface of the wafer 206 has substantially increased over the standard bias voltage. That is, in prior art systems, the applied bias voltage is generally equally applied to both the surface of the top electrode and the surface of the wafer. Thus, by increasing
5 the surface area of the sheath 231 that is proximate to the top electrode 200 surface, it is possible to increase the bias voltage over the surface of wafer 206, while slightly decreasing the bias voltage over the surface of the top electrode 200.

Figure 5 shows a graph illustrating bias vs. area ratio for the plasma sheaths of the top electrode 200 and the wafer 206, assuming that a sinusoidal RF potential is
10 used and proper current balancing is in effect, in accordance with one embodiment of the present invention. When the sheath areas of the top electrode 200 and wafer 206 are about the same, the bias voltage (i.e., Electrode Potential/ V_{peak}) on both the top electrode 200 and wafer 206 will be about -0.3. However, the bias voltage of the top electrode 200 is shown to decrease as the area ratio increases. Conversely, the bias of
15 the wafer 206 is shown to increase as the area ratio increases.

In a preferred embodiment, when the plasma sheath 231 has an area, that is about 2.7 times greater than the area, of the plasma sheath 232, the bias voltage on the wafer 206 will increase to about -0.75, while the bias voltage on the top electrode 200 will decrease to about -0.05. Because the bias voltage is now greater on the surface of
20 the wafer 206, a larger ion bombardment energy will be present on the surface of the wafer 206 to assist in high aspect ratio semiconductor etching operations.

As an advantage, it is now possible to increase the bias voltage over the surface of the wafer 206 without causing an increase in plasma density. As mentioned above, when the plasma density is caused to increase beyond an acceptable

level, the processing gases may fail to perform their desired etching functions. Further yet, because an increased bias voltage is essentially an increase in ion bombardment energy, higher aspect ratio geometries can now be etched without causing premature etch stops, bow etch effects, or process window shifts.

5 In addition, although the above described parameters are associated with chambers configured to process "8 inch wafers," the parameters may be modified for application to substrates of varying sizes and shapes, such as those employed in the manufacture of semiconductor devices and flat panel displays. While this invention has been described in terms of several preferred embodiments, there are alterations, 10 permutations, and equivalents which fall within the scope of this invention. It should also be noted that there are many alternative ways of implementing the methods and apparatuses of the present invention. It is therefore intended that the following appended claims be interpreted as including all such alterations, permutations, and equivalents as fall within the true spirit and scope of the present invention.